REMARKS

Claims 9 and 11 have been previously canceled. Claims 12 and 21 have been amended. Claims 1 through 8, 10, and 12 through 21 remain in the application.

35 U.S.C. § 102

Claims 1, 10, 12, 20, and 21 were rejected under 35 U.S.C. § 102(b) as being anticipated by "Simulation, Animation, and Shop-Floor Control", by Cynthia Erickson et al. Applicants respectfully traverse this rejection.

The publication "Simulation, Animation, and Shop-Floor Control", by Cynthia Erickson et al. discloses that it is often desirable to link shop-floor hardware directly to a discrete-event simulation model or graphical animation. In this case, a simulation model, linked directly to one or more programmable controllers, provides the controller(s) with system scenarios under which they are expected to perform and produce a response. A second application is system emulation, where real-time data is used to drive an animation. Emulation has been used to describe graphical systems displaying the current status of the manufacturing shop floor. Linking a simulation directly to a programmable logic controller (PLC) provides a means to test the control logic of the PLC. Once the control logic for the PLC has been written, it must be debugged and tested. Currently, much of this verification takes place on the shop floor once the manufacturing system is in place. A startup phase is usually planned, during which the manufacturing system operates at low capacity, in order to debug the control software. To verify PLC logic using simulation, a model of the physical system must be developed; however, the timing of some events would be generated by the PLC. Erickson et al. does <u>not</u> disclose a PLC logical verification system dynamically interacting through input and output with a simulation model to verify a PLC code of a manufacturing line.

In contradistinction, independent claim 1 claims the present invention claimed as a method of part flow for a programmable logic controller logical verification system. The method includes the steps of constructing a simulation model of a manufacturing line using a computer, playing the simulation model by a PLC logical verification system on the computer and viewing a flow of a part through the manufacturing line by a user. The PLC logical verification system dynamically interacts through input and output with the simulation model to verify a PLC code of the manufacturing line. The method also includes the steps of determining if the part flow represented in the simulation model is correct to the user and generating PLC code if the part flow represented in the simulation model is correct. The method further includes the steps of using the generated PLC code and implementing the manufacturing line according to the part flow simulation model. Independent claims 12 and 21 have been amended to further include the limitation of <u>viewing a flow of a represented part through the manufacturing line by a user by collecting part locations of the simulation model and coupling the collection of part locations with a part generator</u>.

A rejection grounded on anticipation under 35 U.S.C. § 102 is proper only where the subject matter claimed is identically disclosed or described in a reference. In other words, anticipation requires the presence of a single prior art reference which discloses each and every element of the claimed invention arranged as in the claim. <u>In re Arkley</u>, 455 F.2d 586, 172 U.S.P.Q. 524 (C.C.P.A. 1972); <u>Kalman v. Kimberly-Clark Corp.</u>, 713 F.2d 760, 218 U.S.P.Q. 781 (Fed. Cir. 1983); <u>Lindemann Maschinenfabrik GMBH v. American Hoist & Derrick Co.</u>, 730 F.2d 1452, 221 U.S.P.Q. 481 (Fed. Cir. 1984).

Erickson et al. does <u>not</u> disclose or anticipate the claimed invention of claims 1, 10, 12, 20, and 21. Specifically, Erickson et al. <u>merely</u> discloses linking shop-floor hardware such as programmable controllers directly to a discrete-event simulation model or a graphical

animation using a system emulator. Erickson et al. lacks a PLC logical verification system dynamically interacting through input and output with the simulation model to verify a PLC code of the manufacturing line. In Erickson et al., there is no PLC logical verification system and the simulation model is linked directly with one or more hardware PLCs to test the control logic of the PLC. Also in Erickson et al., one or more hardware PLCs are linked with a system emulator for graphical animation of the manufacturing shop floor. As is known in the art, an emulator represents a physical device in software. (See Wikipedia dictionary definition from Wikipedia website). The PLC logical verification system is not a software representation of a physical device, but a software tool that allows dynamic interaction directly with a simulation model to test PLC logic by having an input and output exchange similar to input/output control logic to validate that the logic is delivering what is intended. The PLC logical verification system analytically verifies the PLC logic. (A similar system is disclosed in U.S. Patent No. 6,442,441). In Erickson et al., the emulator does not allow dynamic interaction directly with a simulation model to test PLC logic to verify a PLC code of the manufacturing line.

As such, Erickson et al. fails to disclose the combination of a method of part flow for a programmable logic controller logical verification system including the steps of constructing a simulation model of a part flow in a manufacturing line using a computer, playing the simulation model by a PLC logical verification system on the computer and viewing a flow of a part through the manufacturing line by a user, wherein the PLC logical verification system dynamically interacts through input and output with the simulation model to verify a PLC code of the manufacturing line, determining if the part flow represented in the simulation model is correct to the user, generating PLC code if the part flow represented in the simulation model is correct, using the generated PLC code, and implementing the manufacturing line according to the part flow simulation model as claimed by Applicants in independent claim 1. In addition, Erickson et

al. fails to disclose the combination of a method of part flow for a programmable logic controller logical verification system of claim 1 including the further limitation of viewing a flow of a represented part through the manufacturing line by a user by collecting part locations of the simulation model and coupling the collection of part locations with a part generator as claimed by Applicants in independent claims 12 and 21. Therefore, it is respectfully submitted that claims 1, 10, 12, 20, and 21 are allowable over the rejection under 35 U.S.C. § 102(b).

35 U.S.C. § 103

Claims 2 through 8 and 13 through 19 were rejected under 35 U.S.C. § 103 as being unpatentable over Erickson et al. in view of "Emulation of a Material Delivery System", by Todd LeBaron and Kelly Thompson. Applicants respectfully traverse this rejection.

As to patentability, 35 U.S.C. § 103 provides that a patent may not be obtained:

> If the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Id.

The United States Supreme Court interpreted the standard for 35 U.S.C. § 103 in Graham v. John Deere, 383 U.S. 1, 148 U.S.P.Q. 459 (1966). In Graham, the Court stated that under 35 U.S.C. § 103:

> The scope and content of the prior art are to be determined; differences between the prior art and the claims at issue are to be ascertained; and the level of ordinary skill in the pertinent art resolved. Against this background, the obviousness or non-obviousness of the subject matter is determined. 148 U.S.P.Q. at 467.

As to the scope and content of the prior art applied by the Examiner, the publication "Simulation, Animation, and Shop-Floor Control", by Cynthia Erickson et al.

discloses that it is often desirable to link shop-floor hardware directly to a discrete-event simulation model or graphical animation. In this case, a simulation model, linked directly to one or more programmable controllers, provides the controller(s) with system scenarios under which they are expected to perform and produce a response. A second application is system emulation, where real-time data is used to drive an animation. Emulation has been used to describe graphical systems displaying the current status of the manufacturing shop floor. Linking a simulation directly to a programmable logic controller (PLC) provides a means to test the control logic of the PLC. Once the control logic for the PLC has been written, it must be debugged and tested. Currently, much of this verification takes place on the shop floor once the manufacturing system is in place. A startup phase is usually planned, during which the manufacturing system operates at low capacity, in order to debug the control software. To verify PLC logic using simulation, a model of the physical system must be developed; however, the timing of some events would be generated by the PLC. Erickson et al. does not disclose a PLC logical verification system dynamically interacting through input and output with a simulation model to verify a PLC code of a manufacturing line.

The publication, "Emulation of a Material Delivery System", by Todd LeBaron and Kelly Thompson, discloses emulation of a complex pick and pack system. A material handling system consists of conveyor sections which continuously move carriers around a closed loop that connects all pick and pack stations. Routing logic, PLC or PC control software, sequencing algorithms and more can be integrated, tested, and debugged within a simulation environment. Emulation has been used for a Rapistan Systems Project to test, debug, and optimize complex algorithms and control logic. Emulation of the Rapistan control system for this project integrates a simulation model with the actual control system. The simulation model provides the output for evaluating control logic and algorithms. The emulation used at Rapistan

Systems was able to prove that the system could handle the projected growth in daily orders. Emulation provides the graphical and statistical output needed to accurately evaluate different algorithms and control logic. LeBaron et al. does not disclose playing a simulation model by a PLC logical verification system on a computer and viewing a flow of a part through the manufacturing line by a user, wherein the PLC logical verification system dynamically interacts through input and output with the simulation model to verify a PLC code of the manufacturing line, and generating the PLC code if a part flow represented in the simulation model is correct. LeBaron et al. also does not disclose determining if the part flow represented in the simulation model is correct to the user. LeBaron et al. further does not disclose using the generated PLC code and implementing the manufacturing line according to the part flow simulation model.

In contradistinction, independent claim 1 claims the present invention as a method of part flow for a programmable logic controller logical verification system. The method includes the steps of constructing a simulation model of a manufacturing line using a computer, playing the simulation model by a PLC logical verification system on the computer and viewing a flow of a part through the manufacturing line by a user. The PLC logical verification system dynamically interacts through input and output with the simulation model to verify a PLC code of the manufacturing line. The method also includes the steps of determining if the part flow represented in the simulation model is correct to the user and generating PLC code if the part flow represented in the simulation model is correct. The method further includes the steps of using the generated PLC code and implementing the manufacturing line according to the part flow simulation model. Independent claims 12 and 21 have been amended to further include the limitation of viewing a flow of a represented part through the manufacturing line by a user by collecting part locations of the simulation model and coupling the collection of part locations with a part generator.

The law followed by our court of review and the Board of Patent Appeals and Interferences is that "[a] prima facie case of obviousness is established when the teachings from the prior art itself would appear to have suggested the claimed subject matter to a person of ordinary skill in the art." In re Rinehart, 531 F.2d 1048, 1051, 189 U.S.P.Q. 143, 147 (C.C.P.A. 1976). See also In re Lalu, 747 F.2d 703, 705, 223 U.S.P.Q. 1257, 1258 (Fed. Cir. 1984) ("In determining whether a case of prima facie obviousness exists, it is necessary to ascertain whether the prior art teachings would appear to be sufficient to one of ordinary skill in the art to suggest making the claimed substitution or other modification.")

As to the differences between the prior art and the claims at issue, Erickson et al. merely discloses linking shop-floor hardware such as programmable controllers directly to a discrete-event simulation model or a graphical animation using a system emulator. Erickson et al. lacks a PLC logical verification system dynamically interacting through input and output with the simulation model to verify a PLC code of the manufacturing line. In Erickson et al., there is no PLC logical verification system and the simulation model is linked directly with one or more hardware PLCs to test the control logic of the PLC. Also in Erickson et al., one or more hardware PLCs are linked with a system emulator for graphical animation of the manufacturing shop floor. As is known in the art, an emulator represents a physical device in software. (See Wikipedia dictionary definition from Wikipedia website). The PLC logical verification system is not a software representation of a physical device, but a software tool that allows dynamic interaction directly with a simulation model to test PLC logic by having an input and output exchange similar to input/output control logic to validate that the logic is delivering what is intended. The PLC logical verification system analytically verifies the PLC logic. (A similar system is disclosed in U.S. Patent No. 6,442,441). In Erickson et al., the emulator does not allow

dynamic interaction directly with a simulation model to test PLC logic to verify a PLC code of the manufacturing line.

LeBaron et al. merely discloses an emulation of a material delivery system in which routing logic, PLC or PC control software, sequencing algorithms and more can be integrated, tested, and debugged within a simulation environment. LeBaron et al. lacks playing a simulation model by a PLC logical verification system on a computer and viewing a flow of a part through the manufacturing line by the user wherein the PLC logical verification system dynamically interacts through input and output with the simulation model to verify a PLC code of the manufacturing line. In LeBaron et al., there is no PLC logical verification system and no PLC code is generated. As is known in the art, an emulator represents a physical device in software. (See Wikipedia dictionary definition from Wikipedia website). The PLC logical verification system is not a software representation of a physical device, but a software tool that allows dynamic interaction directly with a simulation model to test PLC logic by having an input and output exchange similar to input/output control logic to validate that the logic is delivering what is intended. The PLC logical verification system analytically verifies the PLC logic. (A similar system is disclosed in U.S. Patent No. 6,442,441). In LeBaron et al., the emulator does not verify the PLC logic or validate that the logic is delivering what is intended.

LeBaron et al. also lacks using the generated PLC code and implementing the manufacturing line according to the part flow simulation model. In LeBaron et al., while LeBaron et al. mentions PLC or PC control software can be tested and debugged within a simulation environment, there is no part flow for a programmable logic controller logical verification system that is viewed by a user and determining if the part flow represented in the simulation model is correct to the user. Further, in LeBaron et al., there is no generated PLC code that is used in implementing a manufacturing line.

As to a level of ordinary skill in the art, Erickson et al. discloses linking shop-floor hardware such as programmable controllers directly to a discrete-event simulation model or a graphical animation using a system emulator. LeBaron et al. discloses emulation in a delivery system in which routing logic, PLC or PC control software, sequencing algorithms and more can be integrated, tested, and debugged within a simulation environment. There is absolutely no teaching of a level of skill in the programmable logic controller and vehicle manufacturing art that a method of part flow for a programmable logic controller logical verification system includes playing a simulation model by a PLC logical verification system on a computer and viewing a flow of a part through the manufacturing line by a user wherein the PLC logical verification system dynamically interacts through input and output with the simulation model to verify a PLC code of the manufacturing line. The Examiner may not, because he doubts that the invention is patentable, resort to speculation, unfounded assumptions or hindsight reconstruction to supply deficiencies in the factual basis. See In re Warner, 379 F. 2d 1011, 154 U.S.P.Q. 173 (C.C.P.A. 1967).

The present invention sets forth a unique and non-obvious combination of a method of part flow for a programmable logic controller logical verification system that allows both the controls developer and the information integrator to use the same part flow model present in the VPLC, resulting in substantial cost and time savings. As such, the references, if combinable, fail to render obvious the combination of a method of part flow for a programmable logic controller logical verification system including the steps of constructing a simulation model of a part flow in a manufacturing line using a computer, playing the simulation model by a PLC logical verification system on the computer and viewing a flow of a part through the manufacturing line by a user, wherein the PLC logical verification system dynamically interacts through input and output with the simulation model to verify a PLC code of the manufacturing

line, determining if the part flow represented in the simulation model is correct to the user, generating PLC code if the part flow represented in the simulation model is correct, using the generated PLC code, and implementing the manufacturing line according to the part flow simulation model as claimed by Applicants in independent claim 1. In addition, Erickson et al. fails to disclose the combination of a method of part flow for a programmable logic controller logical verification system of claim 1 including the further limitation of viewing a flow of a represented part through the manufacturing line by a user by collecting part locations of the simulation model and coupling the collection of part locations with a part generator as claimed by Applicants in independent claims 12 and 21.

Further, the CAFC has held that "[t]he mere fact that prior art could be so modified would not have made the modification obvious unless the prior art suggested the desirability of the modification". In re Gordon, 733 F.2d 900, 902, 221 U.S.P.Q. 1125, 1127 (Fed. Cir. 1984). The Examiner has failed to show how the prior art suggested the desirability of modification to achieve Applicants' invention. Thus, the Examiner has failed to establish a case of prima facie obviousness. Therefore, it is respectfully submitted that claims 2 through 8 and 13 through 19 are allowable over the rejection under 35 U.S.C. § 103.

Obviousness under § 103 is a legal conclusion based on factual evidence (In re Fine, 837 F.2d 1071, 1073, 5 U.S.P.Q.2d 1596, 1598 (Fed. Cir. 1988), and the subjective opinion of the Examiner as to what is or is not obvious, without evidence in support thereof, does not suffice. Since the Examiner has not provided a sufficient factual basis, which is supportive of his/her position (see In re Warner, 379 F.2d 1011, 1017, 154 U.S.P.Q. 173, 178 (C.C.P.A. 1967), cert. denied, 389 U.S. 1057 (1968)), the rejection of claims 2 through 8 and 13 through 19 is improper. Therefore, it is respectfully submitted that claims 2 through 8 and 13 through 19 are allowable over the rejection under 35 U.S.C. § 103.

Based on the above, it is respectfully submitted that the claims are in a condition for allowance or in better form for appeal. Applicants respectfully request reconsideration of the claims and withdrawal of the final rejection. It is respectfully requested that this Amendment be entered under 37 C.F.R. 1.116.

Respectfully submitted,

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